

## REMARKS

In accordance with the provisions of 37 CFR 1.114, removal of the finality of the Office Action March 11, 2003 and examination of the amended claims presented herewith is respectfully requested.

Appreciation is expressed to the Examiner for the allowance of claim 19 and 22 and the indication of allowable subject matter in claim 26.

By the present amendment, claim 26 has been rewritten into independent form to incorporate all limitations of its parent claim 25 to place it in condition for allowance in light of the Examiner's indication of allowable subject matter.

Also by the present amendment, independent claim 17, 25 and 27 have been amended to clarify the invention, with appropriate changes being made to their respective dependent claims. In addition, claims 31-35 have been deleted, without prejudice to the applicants' right to proceed with seeking patent protection on the subject matter of these claims in a continuation application. New dependent claims 36-38 have been added to further define the invention.

Reconsideration and allowance of amended independent claims 17 and 25, and their respective dependent claims over the asserted prior art to Mizuno is respectfully requested. As discussed in the amendment filed on January 28, 2003, a significant distinction of the present claims over the Mizuno reference is that the present invention controls all three elements of the operating frequency of the clock signal, the supply voltage Vdd and the substrate bias voltage Vbb, as discussed for example, on page 4, line 3, et seq. In particular, applicants have discovered that by controlling all three of these elements it is possible to obtain improved operating speed and lower power consumption than would otherwise be the case if only two of these variables were controlled (which is conventional). In particular, as discussed

on pages 4 and 11 of the specification and illustrated in Fig. 3, by controlling all three of the elements of the operating frequency of a clock signal, the supply voltage Vdd and a substrate bias voltage Vbb it is possible to design for the typical device characteristics shown in Fig. 3 rather than the worst device characteristics also shown in Fig. 3.

In the present amendment, each of the independent claims 17 and 25 has been amended to further define the control of the three characteristics in order to obtain both improved operating speed and power consumption. In particular, each of the independent claims 17 and 25 now specifically defines that at least one of the three elements of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set to satisfy a predetermined value of one of the operating speed and the power consumption while at least one of the remaining values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are also set to improve the other of the operating speed and the power consumption.

It is respectfully submitted that the Mizuno reference fails to teach or suggest these further defining limitations set forth in the amended claim 17 and 25. At the outset, it is noted that the Office Action specifically recognizes that, with regard to Mizuno:

“Not disclosed by Mizuno et al. is changing the supply voltage in response to the first circuit changing its operating state”.

However, the Office Action goes on to state that it would be obvious to do so since:

“Those having ordinary skill in the art who know that it is common to lower the Vcc voltage when the IC has been idle for a while, and since Mizuno et al. already teach monitoring for such an idle condition (see, e.g., col. 3, lines 50) the lowering Vcc during an idle condition does not represent a patentable distinction over Mizuno et al”.

Applicants respectfully submit the teaching set forth in Mizuno regarding monitoring idle condition does not render the present amended claims 17 and 25 obvious for at least two reasons. The first of these is the fact that the invention defined by claim 17 and 25 operates completely differently than the operation which would occur in Mizuno even if it did operate to lower the supply voltage in response to an idle condition being recognized. In particular, since Mizuno's system is based on controlling the substrate bias voltage, lowering of the power supply would cause a lowering of the operating speed of the circuit. In the present claimed invention set forth in claims 17 and 25, on the other hand, controlling the supply voltage and the substrate voltage are both carried out in order to maintain a desired frequency and an improved power consumption. This is particularly described on page 11, line 15 through page 12, line 4 of the specification with regard to Fig. 3, as follows:

“For example, the main circuit LSI operating on an A point (worst) is controlled through the substrate bias so that it may be operated on an A' point (typical). In this case, the supply voltage may be lowered as keeping the same operating speed or processing speed, thereby greatly reducing the power consumption. Alternatively, the main circuit LSI that is operating on the A point (worst) is controlled through the substrate bias so that it may be operated on an A" point. Also in this case, the operating speed may be raised as keeping the same supply voltage or power consumption. By controlling the substrate bias, the operating clock frequency and the supply voltage as mentioned above, the control point A, B or C of the main circuit LSI may be shifted to the control point A', B' or C' for lowering the power consumption or the control point A", B" or C" for enhancing the operating speed”.

In order to assist the Examiner in better understanding the significance of this difference, a reference figure is provided herewith showing both the operation of Mizuno and the operation of the present invention. As noted above, in Mizuno since only the substrate voltage is controlled, when the frequency is increased the power consumption will also increase. On the other hand, because both substrate voltage

and supply voltage are controlled in accordance with the present invention, when the frequency is increased to the same value which would take place in Mizuno, an increase in power consumption can be suppressed by a corresponding lowering of the supply voltage. This claimed control of both supply voltage and substrate voltage, in combination with control of the frequency, to provide both improved operating speed and power consumption, is complete lacking in Mizuno. Therefore, even if the proposed modification set forth in the Office Action was made with regard to Mizuno, the resulting structure would still fail to teach or suggest the features set forth in amended claim 17 and 25.

In addition, it is also respectfully submitted that the proposed modification set forth in the Office Action goes against the dictates of the CAFC as set forth in both of the cases *In re Lee*, 61 USPQ 2d 1434 (Fed. Cir. 2002) and *In re Fine* 5 USPQ 2d 1596 (Fed. Cir. 1988). In particular, the Office Action relies on speculation as to what would have been obvious to one of ordinary skill in the art with regard to lowering the supply voltage when the IC has been idle for a while. As set forth in the *In re Lee*:

“This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references simply to ‘use that which the inventor taught against its teacher’”. 61 USPQ 2d at 1434.

Similarly, in the case of *In re Fine*, the CAFC warned against modifying references beyond their specification teachings with the statement:

“The Eads and Warnick references disclose, at most, that one skilled in the art might find it obvious to try the claimed invention. But whether a particular combination might be ‘obvious to try’ is not a legitimate test of patentability.” 5 USPQ 2d at 1599.

The court goes on to state:

“Instead, the Examiner relies on hindsight in reaching his obviousness determination. But this court has said, ‘to imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge’ is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher”.

It is respectfully submitted that modifying the Mizuno reference to arrive at the detailed limitations set forth in amended claims 17 and 25 would amount to exactly such a hindsight analysis specifically prohibited by the CAFC in the cases of *In re* Fine and *In re* Lee. Therefore of reconsideration and allowance of the independent claims 17 and 25 is earnestly solicited.

Dependent claims 20 and 21 serve to even further define these distinctions. Specifically, claim 20 further defines claim 17 by specifying that one value of the frequency the clock signal, the supply voltage and the substrate voltage is set to satisfy a predetermined operating speed while the remaining two values are set in order to lower the power consumption of the first circuit. Claim 21 defines the opposite situation of setting one value of the frequency of the clock signal, the supply voltage and substrate bias voltage to satisfy a predetermined power consumption and setting the remaining two values in order to increase the operating speed of the first circuit. As discussed above, this interrelationship between setting of three values in order to improve both power consumption and operating speed is completely lacking from the Mizuno reference. It also involves a complete modification of Mizuno to arrive at these features, complete contrary to the teachings of *In re* Fine and *In re* Lee. For these reasons, particularly consideration and allowance of claims 20 and 21 is also respectfully requested.

Reconsideration and allowance of independent claim 25 is also respectfully requested. Claim 25 is particularly directed to the feature of a second circuit for suppressing variations of the operating frequency of the first circuit by applying a substrate bias voltage in conjunction with setting one of the frequency of the clock signal and the supply voltage of the first circuit whose operating frequency variations are suppressed by the substrate bias voltage, to satisfy the predetermined value of one of the operating speed and the power consumption of the first circuit, while setting the other of the clock frequency and the supply voltage to improve the other of the operating speed and power consumption of the first circuit. Again, this interrelated operation involving all three variables of the clock frequency, the supply voltage and the substrate bias voltage in order to improve both power consumption and operating speed is completely lacking from Mizuno, and, as discussed above, the complete modification of Mizuno that would be required in order to meet these features would amount to a complete hindsight reconstruction which is clearly improper. Therefore reconsideration and allowance of amended claim 25 is also respectfully requested.

Finally, consideration and allowance of the new dependent claims 36-38 is also respectfully requested. These claims each define:

“Wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set by selecting one from combinations of at least two from the frequency of the clock signal, the supply voltage and the substrate bias voltage.”

This feature is also completely lacking from the Mizuno reference. Therefore, consideration and allowance of these newly submitted claims is also earnestly solicited.

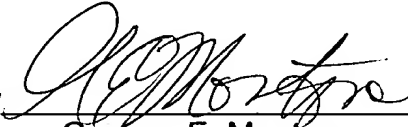
For the reasons set forth above, it is respectfully submitted that all of the pending claims clearly define over the prior cited art, and entry of this amendment and allowance of this application as amended is respectfully requested.

In view of the foregoing, entry of the present amendments and examination of the above-identified application on the merits in due course, are respectfully requested.

Kindly charge any additional fees due, or credit overpayment of fees, to Deposit Account No. 01-2135 (500.39910X00).

Respectfully submitted,

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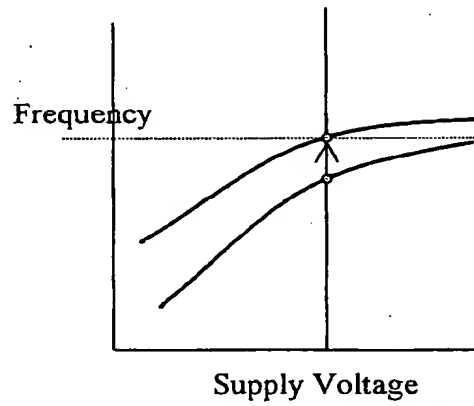
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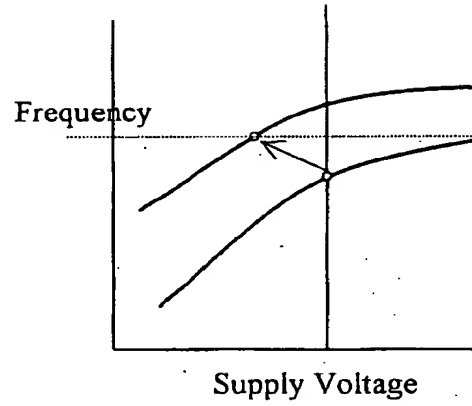
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## Reference Figure

(1) Mizuno



(2) Present invention





**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

The following claims have been amended:

17. (Amended) A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit; and

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed,

wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are adjusted according to an operating performance of the first circuit, and

~~wherein initial values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are decided based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage.~~

wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit,

wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set in order to satisfy a predetermined value of one of the operating speed and the power consumption of the first circuit; and

wherein at least one of a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are set in order to improve another of the operating speed and the power consumption of the first circuit.

20. (Amended) The semiconductor integrated circuit device according to claim 17, ~~wherein the operating performance of the first circuit includes at least on operating speed and a power consumption of the first circuit,~~

wherein one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set in order to satisfy a predetermined operating speed, and

wherein a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are set in order to lower the power consumption of the first circuit.

21. (Amended) The semiconductor integrated circuit device according to claim 17, ~~wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit,~~

wherein one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set in order to satisfy a predetermined power consumption, and

wherein a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are set in order to increase the operating speed of the first circuit.

25. (Amended) A semiconductor integrated circuit device comprising:

- a first circuit including at least one MOS transistor;
- a monitor including at least one MOS transistor;
- a second circuit to control a frequency of a clock signal to be supplied to the first circuit;
- a third circuit to control a supply voltage of the first circuit;
- a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of said first circuit is formed; and

wherein values of the frequency of the clock signal, the supply voltage and the substrate bias voltage value are set initially in order to satisfy an operating performance of the first circuit, ~~based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage, and~~

wherein the clock signal, the supply voltage and the substrate bias voltage are supplied to the monitor, and at least one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is controlled so as to reduce a delay between an output of the monitor and a reference signal.

wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit,

wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is initially set in order to satisfy a predetermined value of one of the operating speed and the power consumption of the first circuit; and

wherein at least one of a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are initially set in order to

improve another of the operating speed and the power consumption of the first circuit.

26. (Amended) The semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a monitor including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit;

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of said first circuit is formed; and

wherein values of the frequency of the clock signal, the supply voltage and the substrate bias voltage value are set initially in order to satisfy an operating performance of the first circuit, based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage, and

wherein the clock signal, the supply voltage and the substrate bias voltage are supplied to the monitor, and at least one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is controlled so as to reduce a delay between an output of the monitor and a reference signal,

a comparator;

wherein the monitor is a delay circuit including inverters connected in series,

wherein the comparator compares an output of the monitor with the reference signal and outputs a first signal when the output of the monitor is later than the

reference signal or a second signal when the reference signal is later than the output of the monitor, and

wherein, when the first signal is outputted, the at least one value is controlled so that the operating speed of the first circuit is made faster, and, when the second signal is outputted, the at least one value is controlled so that the operating speed of the first circuit is made lower.

27. (Amended) A semiconductor integrated circuit device comprising:

a first circuit having a first MOS transistor of a first conductivity type and a second MOS transistor of a second conductivity type connected in series with the first MOS transistor; and

a second circuit to control substrate bias voltages supplied to semiconductor regions where the first and second MOS transistors are formed,

wherein said second circuit suppresses variations of an operating frequency of the first circuit by applying the substrate bias voltage, and

~~wherein a frequency of a clock signal to be supplied to the first circuit and a supply voltage of the first circuit are decided initially for the first circuit whose operating frequency variations are suppressed, based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage.~~

wherein one of a frequency of a clock signal and a supply voltage of the first circuit, whose operating frequency variations are suppressed, are set in order to satisfy a predetermined value of one of the operating speed and the power consumption of the first circuit; and

wherein another of the frequency of the clock signal and the supply voltage of the first circuit is set in order to improve another of the operating speed and the power consumption of the first circuit.